CLAIMS:

1. A method of forming memory circuitry comprising a memory array having a plurality of memory capacitors and comprising peripheral memory circuitry operatively configured to write to and read from the memory array, comprising:

forming a dielectric well forming layer over a semiconductor substrate;

removing a portion of the well forming layer effective to form at least one well within the well forming layer;

forming an array of memory cell capacitors within the well; and

forming the peripheral memory circuitry laterally outward of the well forming layer memory array well.

2. The method of claim 1 wherein the well forming layer consists essentially of doped silicon dioxide.

3. The method of claim 1 wherein the well has a well base which is substantially planar.

4. The method of claim 1 wherein the semiconductor substrate comprises word lines having insulative caps and the well has a well base, the removing leaving a lowest portion of the well base at least 2000 Angstroms above the caps.

5. The method of claim 1 wherein the capacitors respectively comprise a portion which has a container shape.

6. The method of claim 1 wherein the capacitors respectively comprise a portion which has a container shape, the portion being formed to be partially received within the well forming layer beneath the well.

7. A method of forming memory circuitry comprising a memory array having a plurality of memory capacitors and comprising peripheral memory circuitry operatively configured to write to and read from the memory array, comprising:

forming a dielectric well forming layer over a semiconductor substrate;

removing a portion of the well forming layer effective to form at least one well within the well forming layer, the well having a well base;

forming an array of capacitor storage node openings through the well base into the well forming layer over storage node contact locations;

supporting an array of storage node capacitor electrodes within the well and base openings therein by the well forming layer; and

forming the peripheral memory circuitry laterally outward of the well forming layer memory array well.

8. The method of claim 7 wherein the well base is substantially planar.

9. The method of claim 7 wherein the semiconductor substrate comprises word lines having insulative caps, the removing leaving a lowest portion of the well base at least 2000 Angstroms above the caps.

10. The method of claim 7 wherein the capacitors respectively comprise a portion which has a container shape, the portion being formed to be partially received within the well forming layer beneath the well base.

11. A method of forming memory circuitry comprising a memory array having a plurality of memory capacitors and comprising peripheral memory circuitry operatively configured to write to and read from the memory array, comprising:

forming a dielectric well forming layer over a semiconductor substrate;

removing a portion of the well forming layer effective to form at least one well within the well forming layer;

forming a capacitor storage node forming layer within the well;

forming an array of capacitor storage node openings within the capacitor storage node forming layer within the well;

forming capacitor storage node electrode within the capacitor storage node forming layer openings;

after forming the capacitor storage node electrodes, removing at least some of the capacitor storage node forming layer from within the well; and

forming the peripheral memory circuitry laterally outward of the well.

12. The method of claim 11 comprising forming an etch stop layer within the well prior to forming the capacitor storage node forming layer, the removing of at least some of the capacitor storage node forming layer comprising etching using a chemistry which is substantially selective to remove the capacitor storage node forming layer relative to the etch stop layer.

13. The method of claim 11 wherein the well is substantially planar.

14. The method of claim 11 wherein the semiconductor substrate comprises word lines having insulative caps and the well has a well base, the removing leaving a lowest portion of the well base at least 2000 Angstroms above the caps.

15. The method of claim 11 wherein the capacitors respectively comprise a portion which has a container shape, the portion being formed to be partially received within the well forming layer beneath the well.

16. The method of claim 11 comprising removing substantially all of the capacitor storage node forming layer from within the well after forming the capacitor storage node electrodes.

17. The method of claim 11 wherein,

the capacitors respectively comprise a portion which has a container shape, the portion being formed to be partially received within the well forming layer beneath the well; and

removing substantially all of the capacitor storage node forming layer from within the well after forming the capacitor storage node electrodes.

18. A method of forming dynamic random access memory circuitry comprising:

forming an array of word lines over a semiconductive substrate;

forming a substantially planar dielectric well forming layer over the word lines;

etching at least one well into the well forming layer which defines a dynamic random access memory array area within the well and dynamic random access peripheral circuitry area laterally outward of well, the well having a substantially planar base;

depositing a dielectric etch stop layer over the well forming layer laterally outward of and to within the well to less than completely fill the well;

forming a dielectric storage node forming layer over the etch stop layer laterally outward of and to within the well to overfill the well;

etching an array of capacitor storage node openings within the well through the storage node forming layer, through the etch stop layer and into the well forming layer over storage node contact locations;

depositing a capacitor storage node layer over the storage node forming layer to within the capacitor storage node openings to less than completely fill the capacitor storage node openings;

removing the capacitor storage node layer from outwardly of the storage node forming layer effective to form capacitor storage node containers within the capacitor storage node openings in electrical connection with the storage node contact locations, the capacitor storage

node containers having top surfaces received elevationally proximate an outermost surface of the dielectric etch stop layer;

after forming the capacitor storage node containers, etching the capacitor storage node forming layer using the dielectric etch stop layer as an etch stop and exposing lateral outer container surface area of the capacitor containers;

forming a capacitor dielectric layer and a cell electrode layer over the capacitor storage node containers including the outer container surface area of the capacitor containers; and

forming the dynamic random access peripheral memory circuitry laterally outward of the well.

19. The method of claim 18 comprising forming the capacitor storage node containers to have the top surfaces received elevationally above the outermost surface of the dielectric etch stop layer by less than 50 Angstroms.

20. The method of claim 18 wherein the dielectric storage node forming layer is initially formed to be non-planar, and further comprising planarizing the dielectric storage node forming layer prior to etching the array of capacitor storage node openings.

21. The method of claim 18 comprising etching substantially all of the capacitor storage node forming layer from the substrate after forming the capacitor storage node electrodes and before forming the capacitor dielectric layer.

22. A method of forming dynamic random access memory circuitry comprising:

forming an array of word lines over a semiconductive substrate;

forming an array of digit lines over the word lines;

forming a substantially planar dielectric well forming layer over the word lines and digit lines;

etching at least one well into the well forming layer which defines a dynamic random access memory array area within the well and dynamic random access peripheral circuitry area laterally outward of well, the well having a substantially planar base;

depositing a dielectric etch stop layer over the well forming layer laterally outward of and to within the well to less than completely fill the well;

forming a dielectric storage node forming layer over the etch stop layer laterally outward of and to within the well to overfill the well;

planarizing the storage node forming layer while effectively leaving the etch stop layer covered by the storage node forming layer;

etching an array of capacitor storage node openings within the well through the storage node forming layer, through the etch stop layer and into the well forming layer over storage node contact locations;

depositing a capacitor storage node layer over the storage node forming layer to within the capacitor storage node openings to less than completely fill the capacitor storage node openings;

removing the capacitor storage node layer from outwardly of the storage node forming layer effective to form capacitor storage node containers within the capacitor storage node openings in electrical connection with the storage node contact locations, the capacitor storage node containers having top surfaces received elevationally proximate an outermost surface of the dielectric etch stop layer;

after forming the capacitor storage node containers, etching substantially all of the capacitor storage node forming layer from the substrate using the dielectric etch stop layer as an etch stop and exposing lateral outer container surface area of the capacitor containers;

forming a capacitor dielectric layer and a cell electrode layer over the capacitor storage node containers including the outer container surface area of the capacitor containers; and

forming the dynamic random access peripheral memory circuitry laterally outward of the well.

23. The method of claim 22 wherein the well forming layer consists essentially of doped silicon dioxide.

24. The method of claim 22 wherein the well etching leaves the well base at least 1000 Angstroms above outermost tops of the digit lines.

25. The method of claim 22 comprising forming the capacitor storage node containers to have the top surfaces received elevationally above the outermost surface of the dielectric etch stop layer by less than 50 Angstroms.

26. Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the well over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

27. The memory circuitry of claim 26 wherein the base is substantially planar.

28. The memory circuitry of claim 26 wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

29. The memory circuitry of claim 26 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

30. The memory circuitry of claim 26 comprising buried digit lines and wherein the base is substantially planar, and the well base being received at least 1000 Angstroms above outermost tops of the digit lines.

31. The memory circuitry of claim 26 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

32. The memory circuitry of claim 26 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

33. Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer having at least one well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

34. The memory circuitry of claim 33 wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Ångstroms above the caps.

35. The memory circuitry of claim 33 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

36. The memory circuitry of claim 33 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

37. The memory circuitry of claim 33 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

38. Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

39. The memory circuitry of claim 38 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

40. The memory circuitry of claim 38 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

41. The memory circuitry of claim 38 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

42. Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

bit lines received over the word lines;

an insulative layer received over the word lines, the digit lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the well over the word lines and the digit lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

43. The memory circuitry of claim 42 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

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44. The memory circuitry of claim 42 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

45. Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

bit lines received over the word lines;

an insulative layer received over the word lines, the digit lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a substantially planar base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the well, the memory cell storage capacitors respectively comprising a storage node container which is partially received within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

46. The memory circuitry of claim 45 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

47. The memory circuitry of claim 45 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

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